

ATopTech Appoints Jue-Hsien Chern as CEO

Company achieves profitability entering into 2010

Santa Clara, CA – January 10, 2010 — ATopTech, Inc., the technology leader in integrated circuit (IC) physical design solutions addressing the challenges of designing ICs at 65 nanometers and below, has appointed Jue-Hsien Chern as CEO. ATopTech also achieved profitability based on record sales from new customer adoption of Aprisa, the complete netlist to GDSII physical design solution, as well as renewals within existing accounts.

“Now that ATopTech has achieved profitability, we are very pleased that someone with Jue-Hsien’s experience has agreed to take the helm and lead us to the next phase of the company’s development,” said Dr. Ping San Tzeng, ATopTech’s president and chief technology officer. “We look forward to continuing the momentum under his leadership.”

Jue-Hsien brings over twenty years of experience in high technology companies to ATopTech. Prior to joining ATopTech, he was vice president and general manager of the DSM division at Mentor Graphics for nine years. He was at Texas Instruments for 10 years, holding positions as SMTS and branch manager within the Semiconductor Process and Design Center. Jue-Hsien has also served as head of the DSM business unit at Avant! and vice president, engineering, and CTO at Technology Marketing Associates.

“Even in the tough economic environment of this past year, ATopTech has successfully grown its customer base and increased market acceptance for the company’s flagship Aprisa and Apogee solutions,” said Jue-Hsien Chern. “I look forward to working with the team as we further the development of the company and technology to meet our customers’ needs in physical design as we move to even smaller geometries.”

About ATopTech

ATopTech, Inc., is a technology leader in IC physical design. Its Precision Optimization technology offers real design closure at 65 nm and below. The company’s first product family, Aprisa, has extremely close correlation to golden sign-off tools, produces design rule check (DRC)-clean designs, features MCMM optimization at all phases, and offers 10-15 percent better timing and up to 10 percent less standard cell area than existing tools. Use of state-of-the-art

multi-threading and distributed processing technologies speeds up the design process, resulting in unsurpassed project completion times. For more information, see <http://www.atoptech.com>. Aprisa and Apogee are trademarks and ATopTech is a registered trademark of ATopTech, Inc. Any other trademarks or trade names mentioned are the property of their respective owners.

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