

AtopTech's Aprisa, Cuts the Physical Design Time of Sharp's Multimillion-Gate System-on-Chip Design

SoC designers using Aprisa produced the best quality of results with very short turn-around time; used flat design methodology which will be continued on other large SoC designs

Santa Clara, CA—January 23, 2008—ATopTech, Inc. a new electronic design automation (EDA) company tackling today's physical design challenges of integrated circuits (ICs) at 90 nanometers and below, today announced that Sharp Corporation, a major Japanese consumer electronics manufacturer, used ATopTech's Aprisa place and route family of physical design tools to complete the tape-out of a system-on-chip for the consumer market. Using Aprisa enabled Sharp to dramatically shorten the physical design time.

Aprisa is a complete netlist-to-GDSII physical design solution that has already been used successfully in several 65nm tape outs and is currently in active use in several 40nm design efforts. Aprisa, based on ATopTech's Interconnect Centric Precision Optimization technology, offers real design closure at 90nm and below.

On this important multi-million-gate system-on-chip (SoC) design, Sharp's goal was to use a flat physical design methodology. Before purchasing Aprisa, the design team was using an industry-standard place and route system, but encountered run time and capacity limitations that prevented the use of a flat design methodology. As a result, Aprisa was purchased, which enabled the design to be done flat, and the design team was able to finish-the high quality SoC in a short turn around time

"Aprisa is a high quality place and route solution," said Mr. Takayoshi Tanaka, General Manager of Development Department III Electronic Components and Devices Development Group, at Sharp Corporation. "We achieved much better design results – in terms of timing, power, and area – and completed the physical design much sooner than we expected. It was gratifying to see that the flat design approach is still feasible for large SoC designs."

"Sharp has a long history of innovation in consumer electronics, and we're pleased that Aprisa was instrumental in the success of their new system-on-chip," said Eddie Araki, President, ATopTech KK. "Sharp's experience with Aprisa in achieving faster time to market, lower design costs, and a better performing product confirms the market need for

our next-generation place and route product family. We look forward to a productive long term relationship with Sharp.”

About Sharp

Sharp Corporation is a worldwide developer of innovative products and core technologies that play a key role in shaping the future of electronics. As a leader in liquid crystal displays (LCDs) and digital technologies, Sharp offers one of the broadest and most advanced lines of consumer electronics, information products and electronic components, while also creating new network businesses. For more information, please visit Sharp's Web site at <http://sharp-world.com/index.html>

About ATopTech

ATopTech Inc. is a technology leader in IC physical design. Its Precision Optimization technology offers real design closure at 90nm and below. The company's first product family, Aprisa, has extremely close correlation to golden sign-off tools, produces design rule check (DRC)-clean designs, 10-15% better timing and up to 10 percent less standard cell area than existing tools. ATopTech Inc. was founded 2003 by Kaiwin Lee PhD, and Don-Min Tsou Ph.D., who with their team are some of the most experienced and successful developers of commercial physical design tools in the world. For more information, see <http://www.atoptech.com>.

All trademarks or trade names mentioned are the property of their respective owners.

#

Editorial Contact:

Michelle Clancy, Cayenne Communication LLC -- 252-940-0981, michelle.clancy@cayennecom.com