

## **ATopTech's Aprisa Physical Design Solution Qualified by TSMC for 40nm Designs**

Santa Clara, CA – January 19, 2010 — ATopTech, Inc., the primary technology leader in integrated circuit (IC) physical design solutions addressing the challenges of designing ICs at 65 nanometers and below, today announced that [Aprisa](#), the company's award-winning physical design solution, has been qualified for TSMC's 40nm technology node, meeting the foundry's requirements of placement, routing and transparent half node implementation.

Aprisa is a complete netlist-to-GDSII physical design solution, including floorplanning, placement, clock-tree synthesis and optimization, global and detailed routing, and an advanced, extremely fast timing engine to solve the complex timing issues associated with on chip variation (OCV) and multi-corner, multi-mode (MCMM) analysis.

Based on ATopTech's Precision Optimization technology, Aprisa enables real design closure at smaller geometries through accurate timing correlation to industry sign-off tools. Aprisa uses state-of-the-art multi-threading and distributed processing technology to further speed up the process and avoid the exploding runtime issues associated with the variability in sub-micron designs.

“We have been pleased to work with ATopTech to qualify their digital implementation tools,” said S. T. Juang, senior director of Design Infrastructure Marketing at TSMC. “We look forward to continuing the collaboration to qualify Aprisa for the next technology node.”

“Aprisa has been successfully used by our customers in multiple 40nm design tapeouts,” said Dr. Ping-San Tzeng, ATopTech President and CTO. “Qualification by TSMC further confirms that our tools are production-ready for 40nm technologies, and gives customers even greater confidence that they can use Aprisa at this node and get excellent results.”

## **About ATopTech**

ATopTech, Inc., is a technology leader in IC physical design. Its Precision Optimization technology offers real design closure at 65 nm and below. The company's first product family, Aprisa, has extremely accurate correlation to golden sign-off tools, produces design rule check (DRC)-clean designs, features MCMM optimization at all phases, and offers 10-15 percent better timing and up to 10 percent less standard cell area than existing tools. The use of state-of-the-art multi-threading and distributed processing technologies speeds up the design process, resulting in unsurpassed project completion times. For more information, see [www.atoptech.com](http://www.atoptech.com)

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