

Design teams, attempting to design the next-generation of complex nanoscale (sub-100 nanometer) chips, face several crises. Challenges such as Signal Integrity, OCV, and Multi-Corner Multi Mode timing, and Leakage Power make it much more difficult to achieve design closure (matching physical results such as timing, dies size, and power to those of the design specification), radically increasing design turnaround times and thus hugely escalating the cost.

In the days of half-micron and above, interconnect could still be, for most practical purposes, ignored. Below half-micron these effects began to require careful consideration (wire-load models), and at 0.18 $\mu$ m (180nm) interconnect delay became such a driving factor in chip performance that topology (placement information) had to be considered during logic design.

At 90nm and below, nanoscale chip behavior drives a critical need to consider numerous complex issues, including precision delay calculation, signal integrity/crosstalk, and power. Process variations become significant even across individual die and can affect timing closure, making it critical to additionally account for on-chip delay variation (OCV). This variability also compounds the problem of optimization for worst- and best-case variations in process, voltage, and temperature (PVT). Variations in parasitic resistance and capacitance complicate traditional “min/max” analysis, creating a matrix of “corner cases” which must be analyzed. Circuit behavior may also change based on chip operating mode (standby vs. active, scan vs. functional, etc.). Thus the ability to do multi-corner, multi-mode analysis becomes very important.

As design teams have neared nanoscale geometries, tool vendors and users have developed a number of techniques to compensate for the deficiencies in the existing tools. Vendors typically use larger capacitance estimations (to add pessimism) while users will try techniques such as “margining” (adding a certain percentage of the clock cycle to the design constraints during placement). Unfortunately, these techniques all usually lead to much more pessimistic designs, meaning higher cell counts, increased area and power, with much longer run times. Indeed, manual intervention is often required to finalize timing paths and achieve timing closure because the current tools addressing these issues do not match up with sign-off tools. Clearly, the “design gap” between designer productivity and product complexity is worsening as silicon manufacturing technologies cross the nanoscale boundary.

Aprisa, the new place and route solution from ATopTech, for the first time incorporates many advanced technologies to achieve true design closure:

- Utilizes sign-off quality engines in an implementation tool. Aprisa has a very accurate multi-threaded 2.5D RC extractor and next generation 'implementation' timing/SI engine with very accurate correlation to all the industry standard sign-off tools such as StarRC, PrimeTime, PrimeTime-SI and CeltIC. A built in DRC engine correlates to sign-off tools such as Calibre. (TM's on these tool names)

## Crossing the Nanoscale Boundary - A Crisis in Chip Design

- Utilizes near detail route parasitics in early stages of the physical design in order to do accurate optimization and addressing problems like signal integrity much earlier in the cycle.
- Utilizes a multi-corner multi-mode timing engine to consider/resolve variability issues.
- Combines powerful place / route / optimization engines working together seamlessly with the precise analysis engines to achieve the best results.

For more information on Aprisa see [www.atoptech.com/products.html](http://www.atoptech.com/products.html)