

Pioneers in Breakthrough IC Design Tools Launch New Company, Announce Proven Physical Design Product

With multimillion-dollar revenues, ATopTech is the new face of physical design for semiconductors at 90nm and below

Santa Clara, Calif., December 10, 2007 –ATopTech, a new electronic design automation (EDA) company, today launched the company and unveiled a new product with new technology for the physical design of integrated circuits (ICs) at 90 nanometers and below.

The new company, ATopTech Inc., was formed in late 2003 and development on the EDA software was begun in 2004. The company has raised \$14 million in two rounds of funding. Investors include the founding team, Acorn Campus Fund II, VCEDA, iD Innovation, Inc., and H&Q.

Founders include Don-Min Tsou, PhD, president; and Kaiwin Lee, PhD, executive officer. Rounding out the executive team are Ping-San Tzeng, PhD, chief architect; Eric Thune, vice president of sales and marketing; and Eddie Araki, President of ATopTech KK in Japan. Members of the Board of Directors are Don-Min Tsou, Kaiwin Lee, and Wu-fu Chen, managing member and co-founder of Acorn Campus.

The ATopTech development team is comprised of the most experienced in the industry, with majority of them having more than 10 years of experience developing physical design toolsets. For several members of the team, this is their third commercial place and route system.

ATopTech's new IC physical design product family, Aprisa, was quietly released in December 2006 and is already generating multiple millions of dollars in revenue. Aprisa has five tapeouts on record, having been used on both 90 and 65nm designs in applications such as network processors and digital video chips. Over 10 more designs are under development at nodes between 65 - 40 nm.

Atiq Raza, founder and chairman of the board of RMI, said, "RMI has benefited considerably from ATopTech's state of the art EDA technology in the development of our products. As RMI builds solutions for the evolving connectivity infrastructure from

the data center to the home, we look forward to utilizing ATopTech's innovations to their full potential."

"As the semiconductor industry moves to technologies at 65 nm and below, the older generation of physical design tools are breaking," said Kaiwin Lee, ATopTech co-founder and executive officer. "Physical design tools created for previous generations of chips simply didn't have to address the challenges of designing chips below 90 nanometers. That's why we started from scratch to design a completely new tool."

At 65 nanometers, designers encounter new challenges such as on-chip variation, multi-corner/multi-mode (MCMM), an increase in crosstalk than previous nodes, and much more complex design rules.

"Chip design issues have become acute problems for semiconductor companies," said Don-Min Tsou, ATopTech co-founder and president. "Schedules are slipping because the turn around time for designs has exploded, and the complexity of design rules has challenged the current generation of tools. Timing no longer correlates to sign-off tools, so timing closure has become a manual task. A minor change near the end of a design can be disastrous. Aprisa takes a giant leap forward in solving these problems."

More About Aprisa

Aprisa is a complete netlist-to-GDSII physical design solution that includes floorplanning, placement, clock tree synthesis (CTS), global routing, and detailed routing. Aprisa is compatible with all industry standards. Customers using Aprisa have reported faster design closure and turn-around time, much fewer buffers, and lower power consumption than with other physical design tools. Timing closure was achieved without extensive manual effort.

Aprisa includes ATopTech's new Interconnect Centric "Precision Optimization" technology, which offers true design closure for designs at 90nm and below. Precision Optimization uses very accurate parasitics (resistance and capacitance) and precise signal integrity analysis, as opposed to other physical design systems, which use estimated parasitic information and margins to compensate for older architectures. Precision

Optimization runs throughout the physical design flow -- during placement, CTS, global and detailed routing.

In addition, Aprisa offers sophisticated parallel computing with features such as concurrent MCMM, multithreading and multiprocessing, with results up to five times faster than existing tools. Aprisa has a small memory footprint enabling very large capacity. The user interface is very easy to use and enables designers to learn to use the tool effectively in a very short period of time. .

Price and Availability

Aprisa is available now. U.S. pricing starts at \$795,000 for a one year time-based license.

About ATopTech

ATopTech Inc. is a technology leader in IC physical design. Its Precision Optimization technology offers real design closure at 90nm and below. The company's first product family, Aprisa, has extremely close correlation to golden sign-off tools, produces design rule check (DRC)-clean designs, 10-15% better timing and up to 10 percent less standard cell area than existing tools. ATopTech Inc. was founded 2003 by Kaiwin Lee PhD, and Don-Min Tsou PhD, who with their team are some of the most experienced and successful developers of commercial physical design tools in the world. For more information, see <http://www.atoptech.com>.

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